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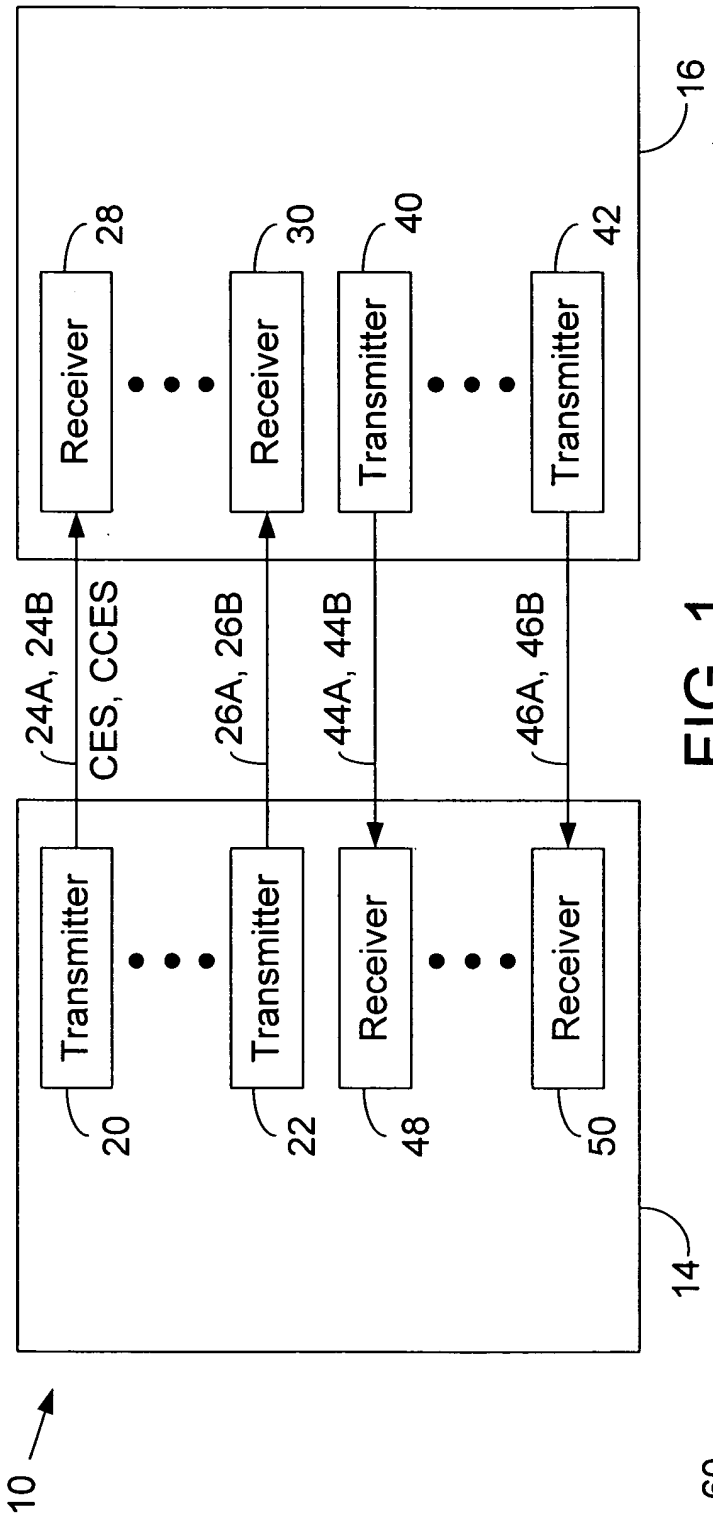

FIG. 1

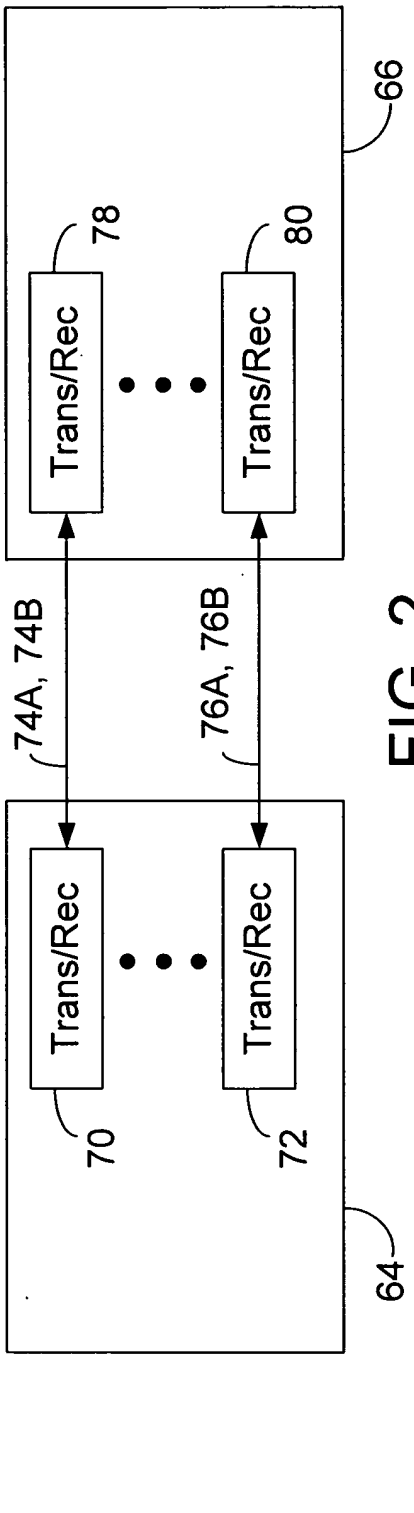

FIG. 2

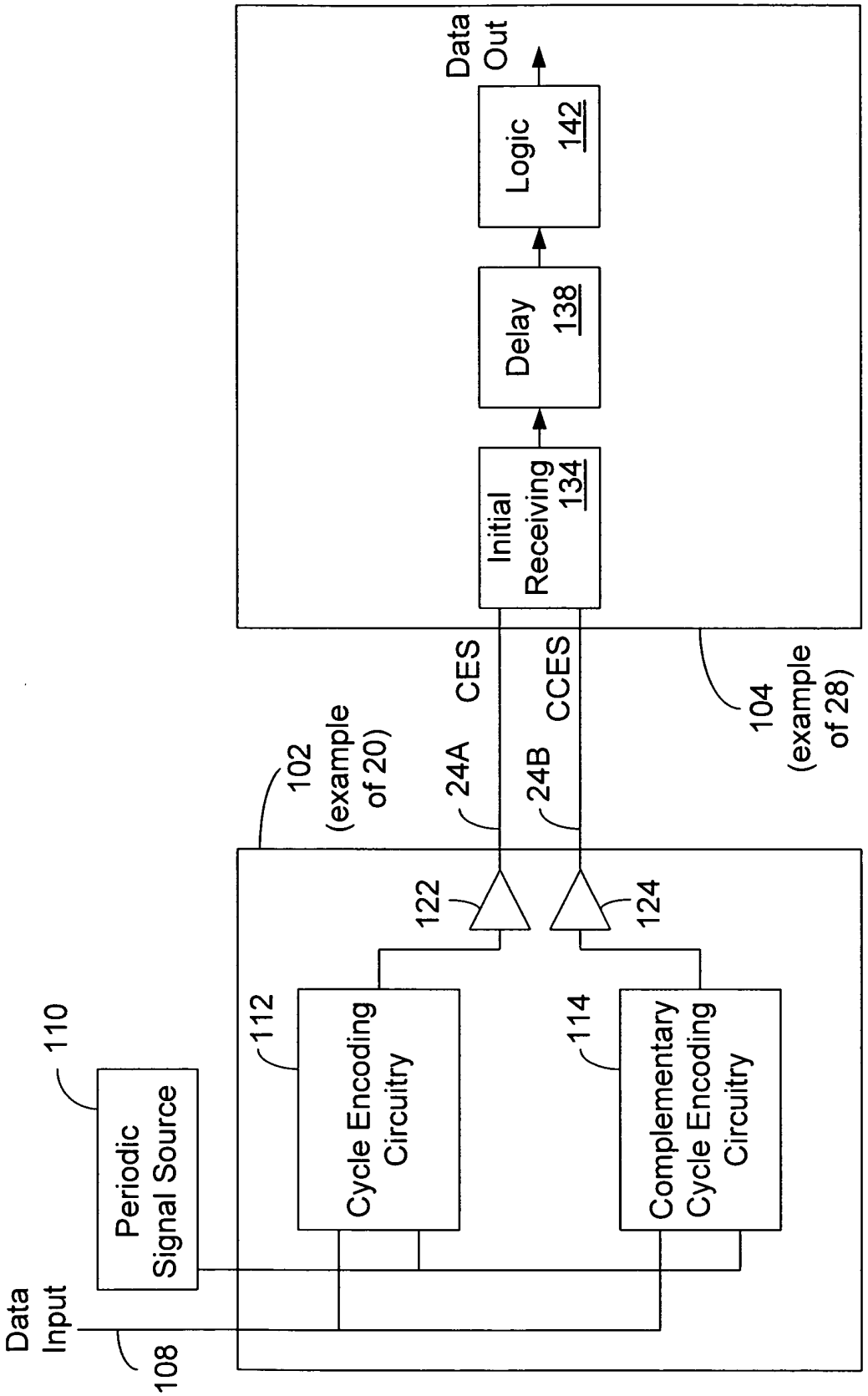
Data Out
Logic 142
Delay 138
Initial Receiving 134
CES
CCES
104 (example of 28)
102 (example of 20)
24A
24B
122
124
112
Cycle Encoding Circuitry
114
Complementary Cycle Encoding Circuitry
110
Periodic Signal Source
Data Input
108

FIG. 3

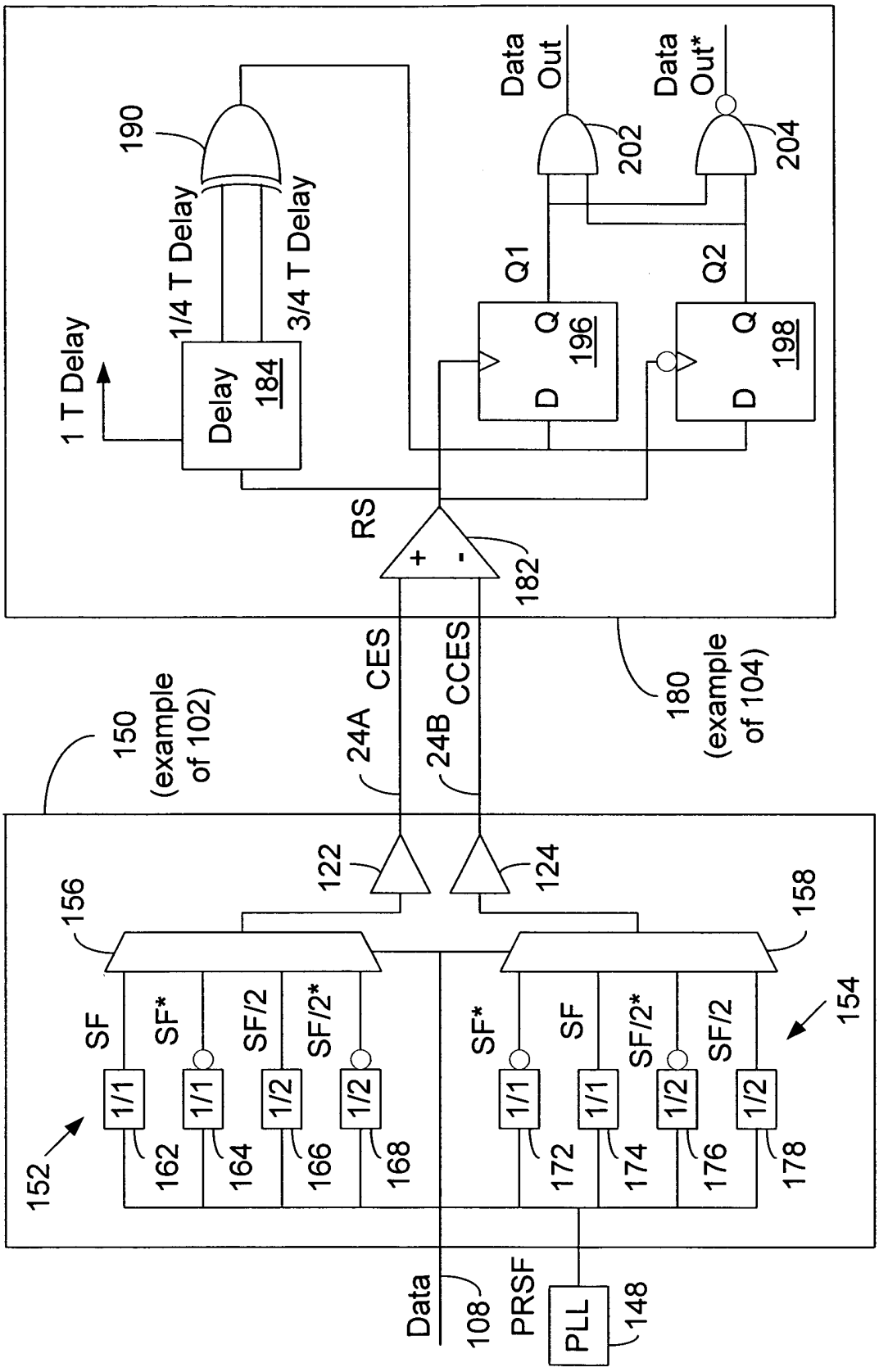
190
1/4 T Delay
3/4 T Delay
1 T Delay
Delay 184
Data Out
Data Out*
202
204
Q1
Q2
Q 196
Q 198
D
D
RS
+
-
182
CES 24A
CCES 24B
180 (example of 104)
150 (example of 102)
122
124
156
158
154
SF
SF*
SF/2
SF/2*
1/1
1/2
152
162
164
166
168
172
174
176
178
Data 108
PRSF
PLL 148

FIG. 4

Data	Signal in previous segment	Signal in response to data
0		
0		
0		
0		
1		
1		
1		
1		

FIG. 6

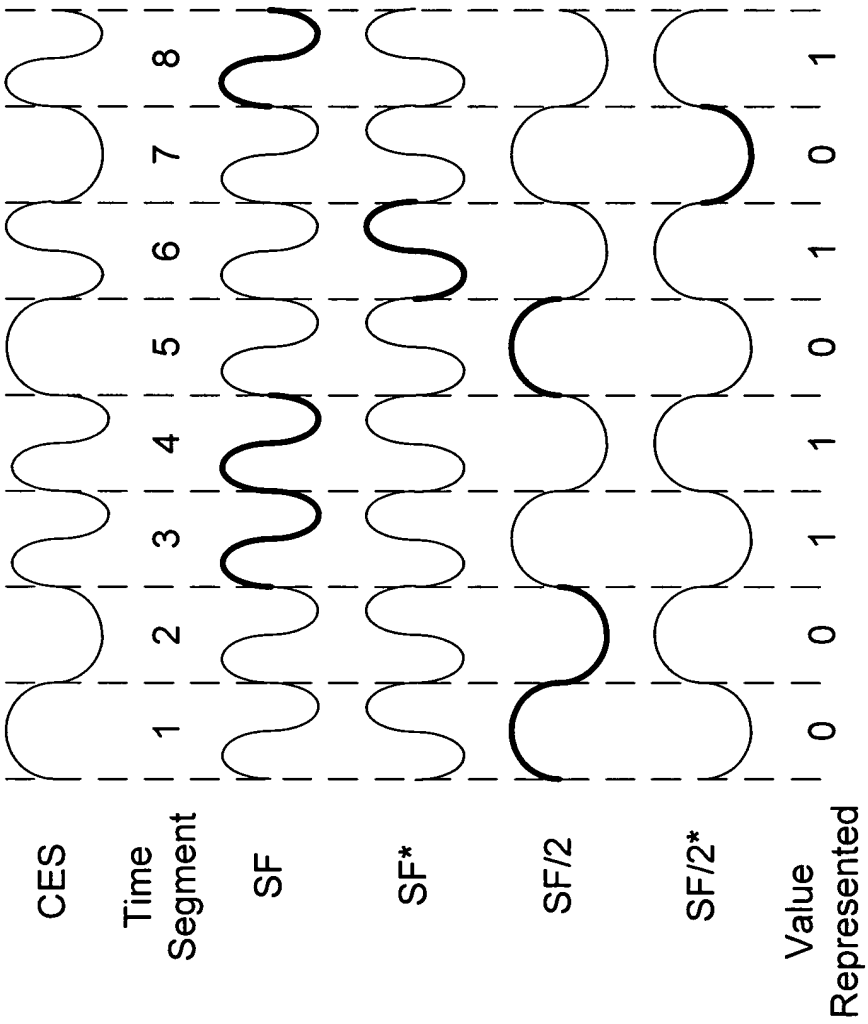

FIG. 5

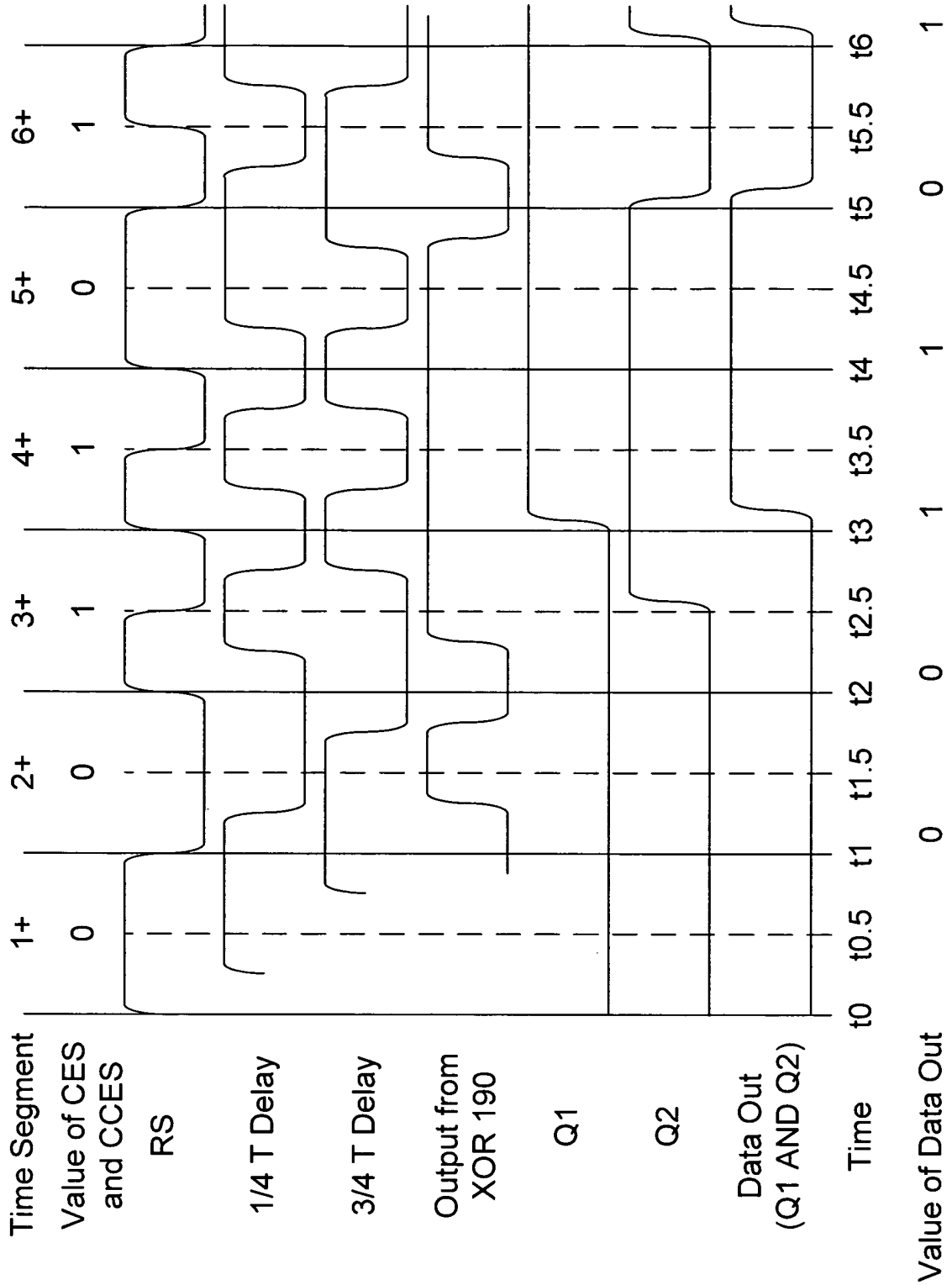
Time Segment
Value of CES and CCES
RS
1/4 T Delay
3/4 T Delay
Output from XOR 190
Q1
Q2
Data Out (Q1 AND Q2)
Time
Value of Data Out
1+
2+
3+
4+
5+
6+
0
1
0
1
0
1
t0
t0.5
t1
t1.5
t2
t2.5
t3
t3.5
t4
t4.5
t5
t5.5
t6
0
0
1
1
0
1

FIG. 7

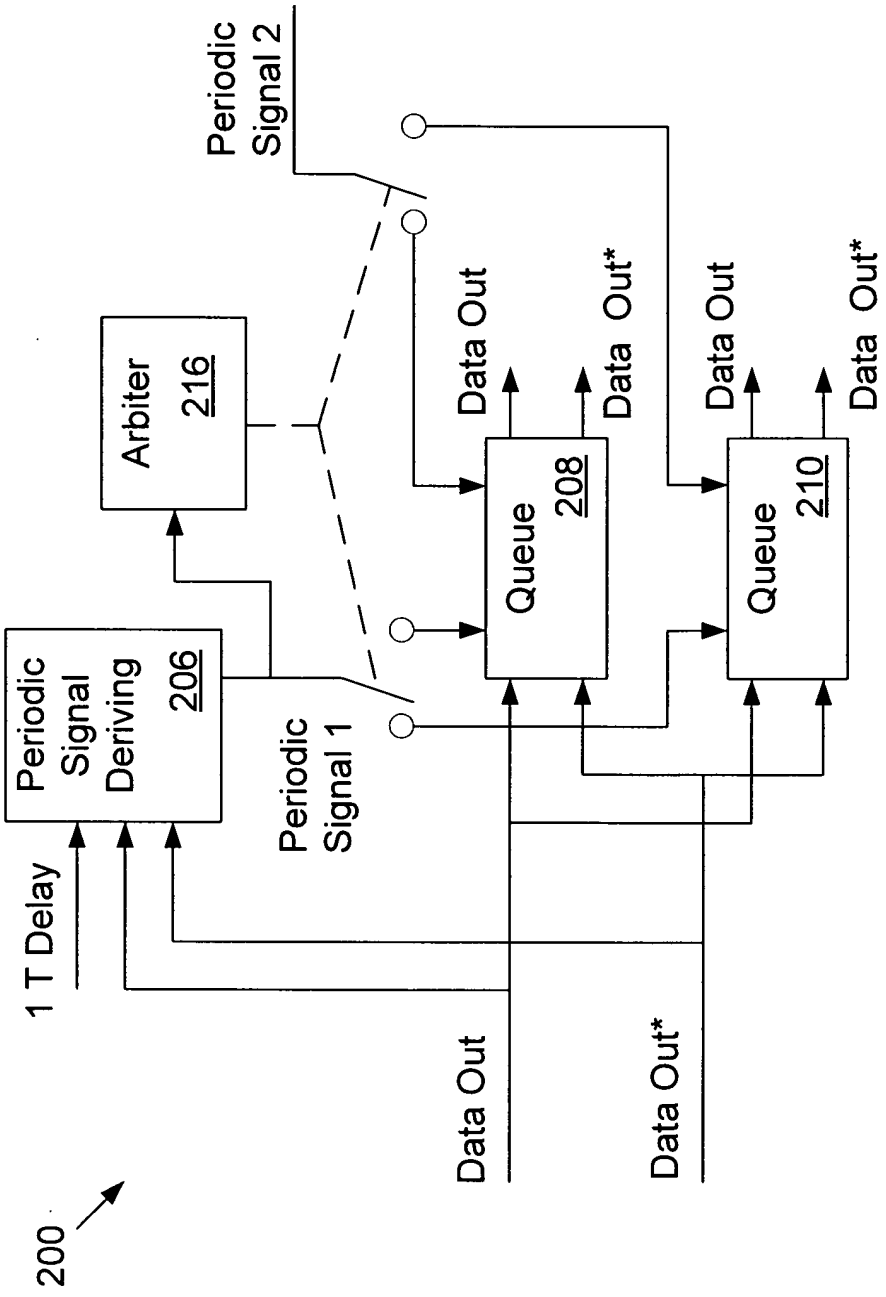
Periodic Signal 2
Arbiter 216
Data Out
Data Out*
Data Out
Data Out*
Queue 208
Queue 210
Periodic Signal Deriving 206
Periodic Signal 1
1 T Delay
Data Out
Data Out*
200

FIG. 8

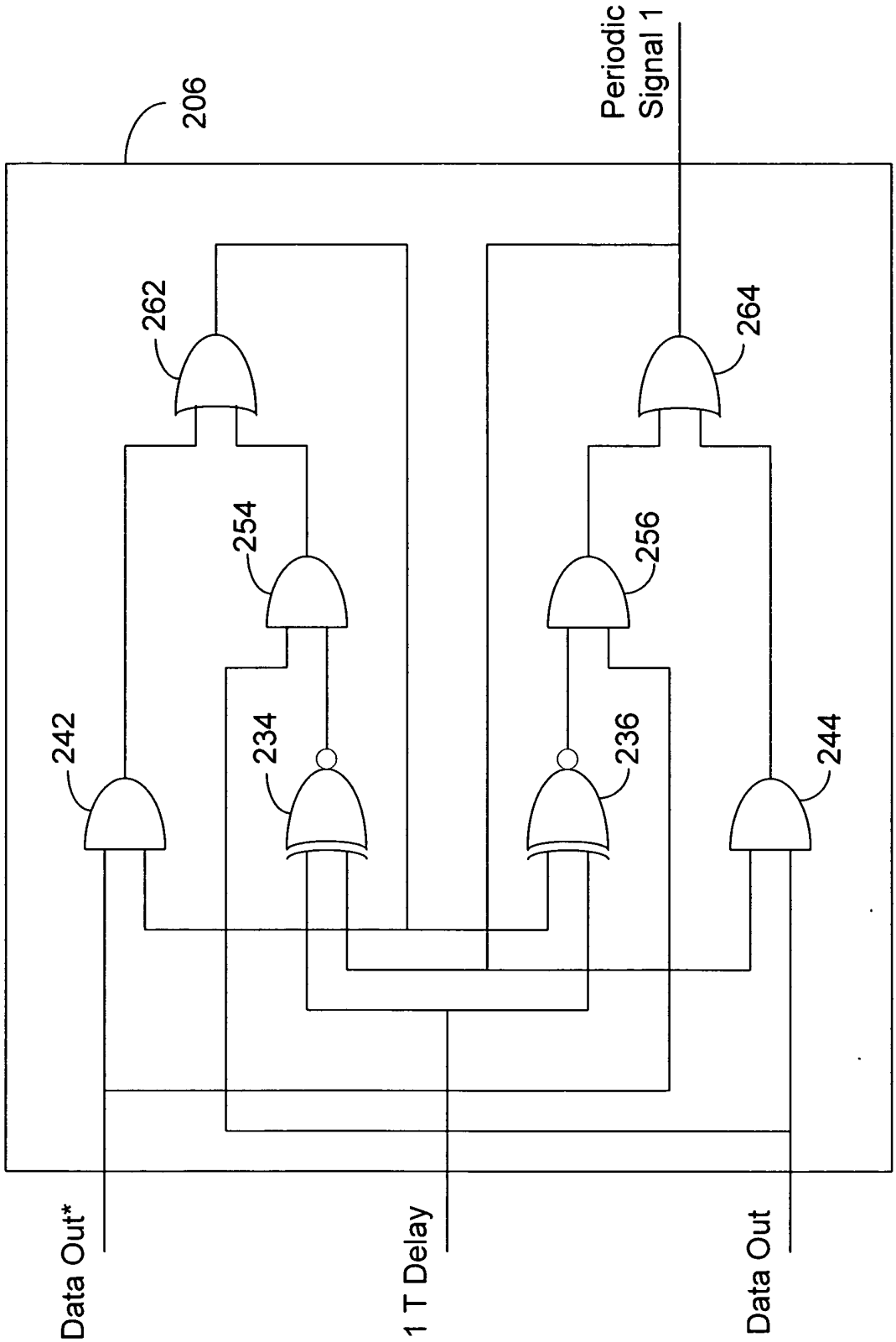
206
Periodic Signal 1
262
264
254
256
242
234
236
244
Data Out*
1 T Delay
Data Out

FIG. 9

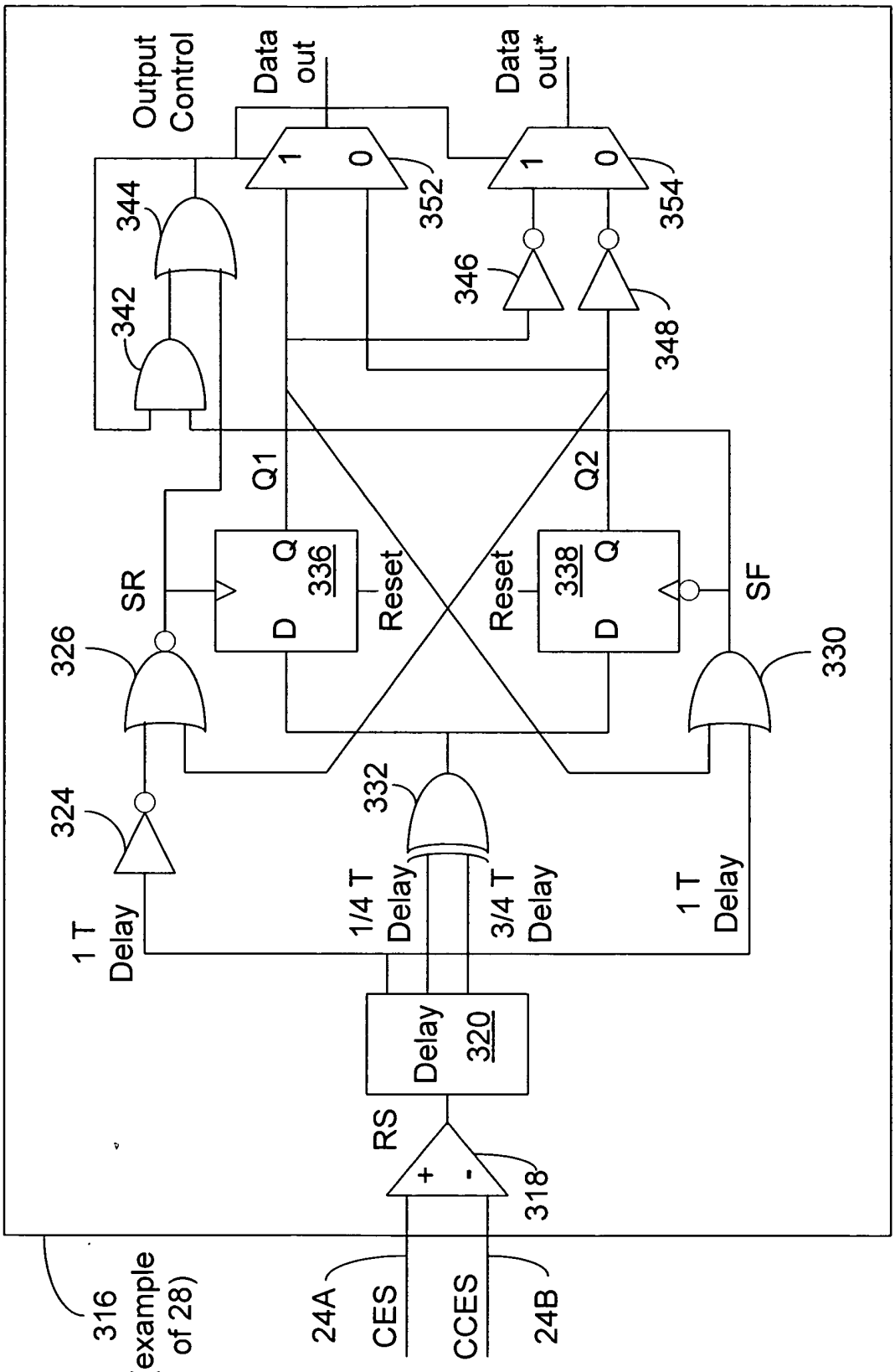
Output Control
Data out
Data out*
344
342
352
354
346
348
Q1
Q2
SR
SF
D
Q
336
338
Reset
326
330
324
332
1 T Delay
1/4 T Delay
3/4 T Delay
1 T Delay
Delay
320
RS
+
-
318
316 (example of 28)
24A
CES
CCES
24B

FIG. 10

Replacement Sheet

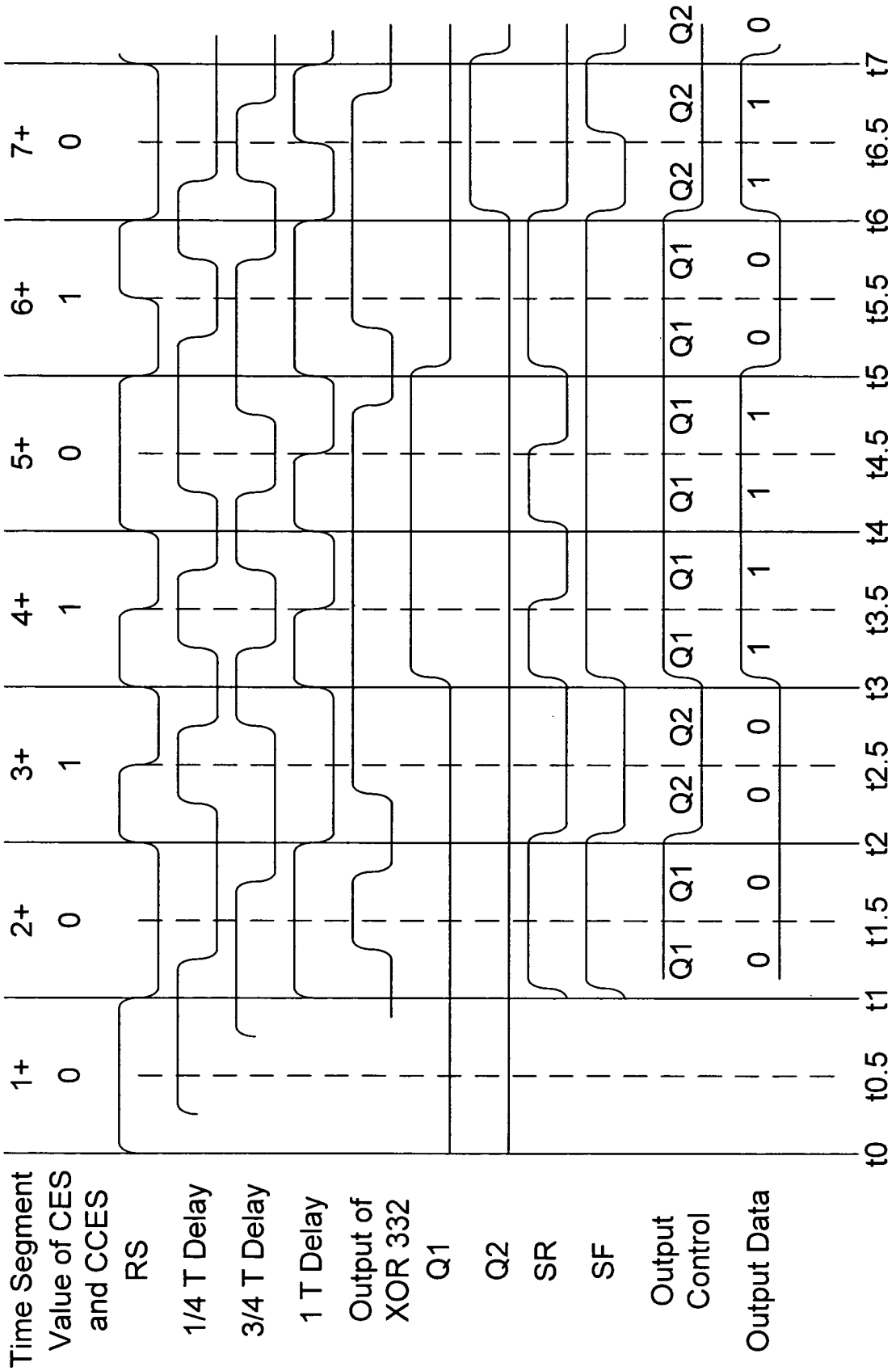

FIG. 11

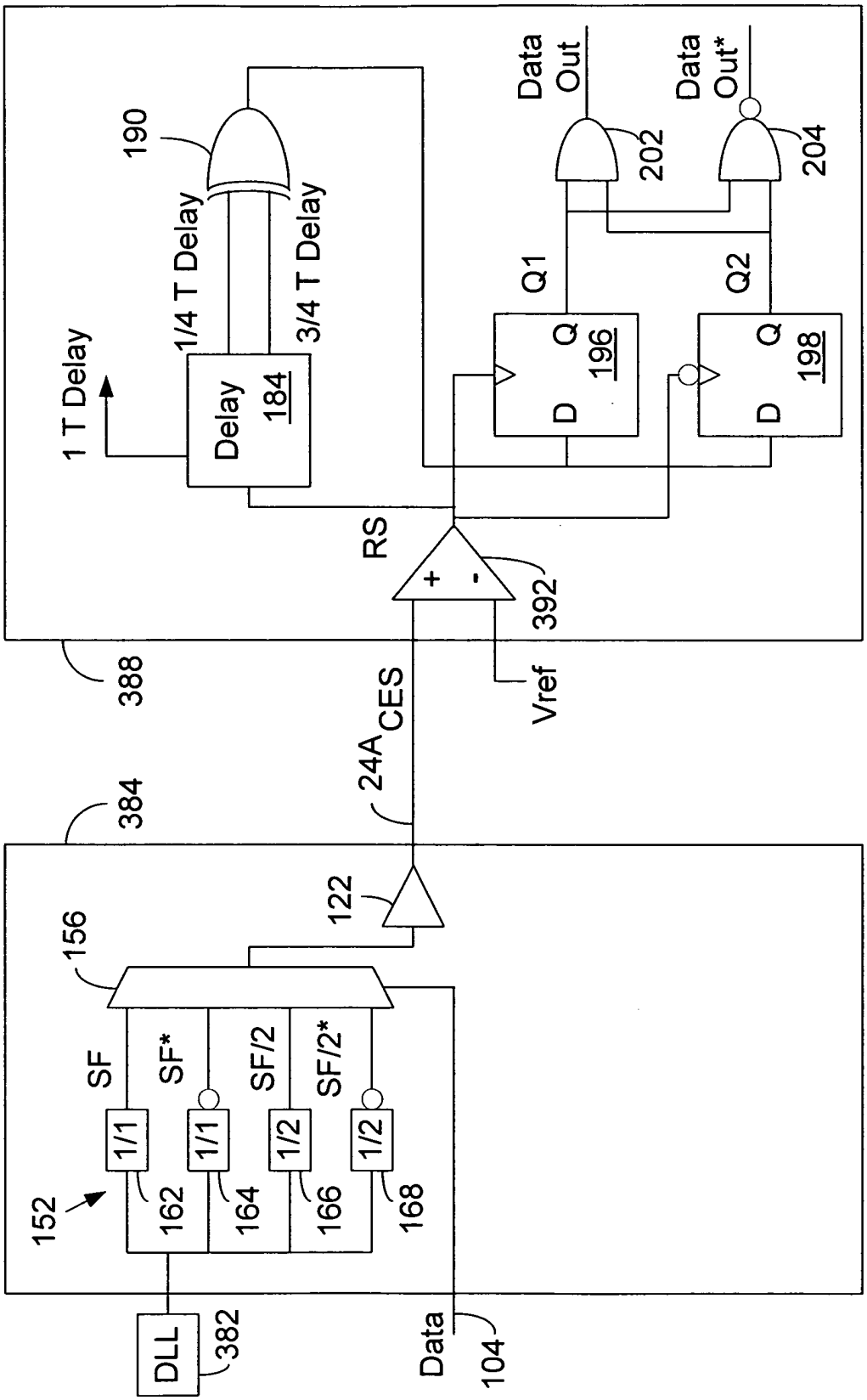
190
1/4 T Delay
3/4 T Delay
1 T Delay
Delay
184
Data Out
Data Out*
202
204
Q1
Q2
Q
D
196
198
RS
+
-
392
388
Vref
CES
24A
384
122
156
SF
SF*
SF/2
SF/2*
1/1
1/2
152
162
164
166
168
DLL
382
Data
104

FIG. 12

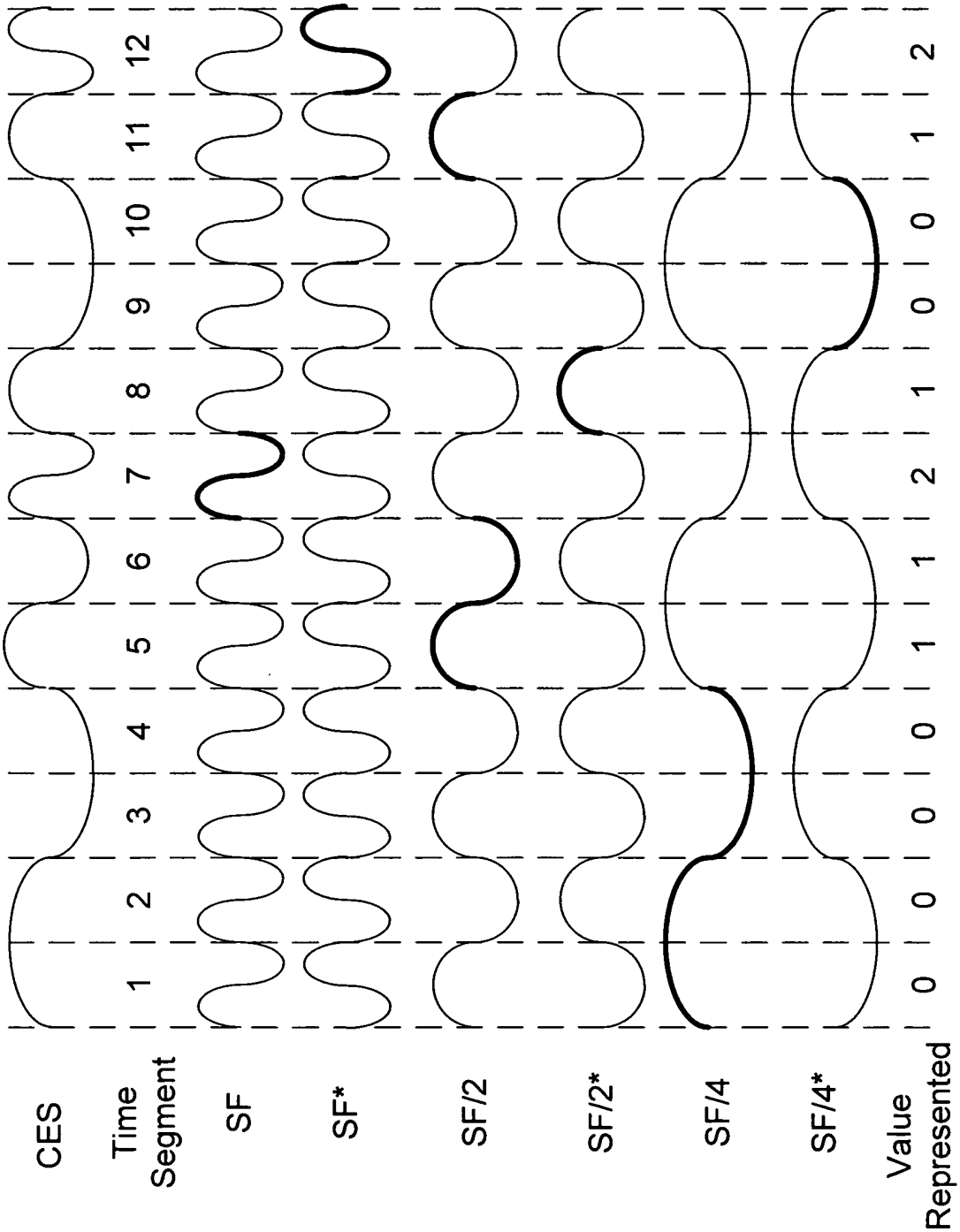
CES
Time Segment
1 2 3 4 5 6 7 8 9 10 11 12
SF
SF*
SF/2
SF/2*
SF/4
SF/4*
Value Represented
0 0 0 0 1 1 2 1 0 0 1 2

FIG. 13

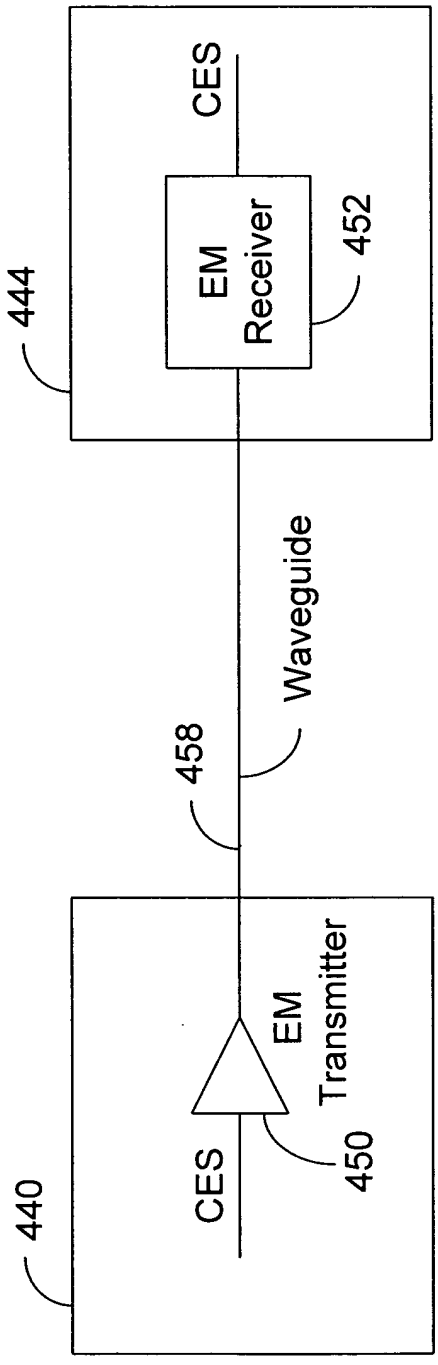
444
CES
EM Receiver
452
458
Waveguide
440
CES
EM Transmitter
450

FIG. 14

474
CES
EM Receiver
478
470
CES
EM Transmitter
476

FIG. 15